

FIG. 1

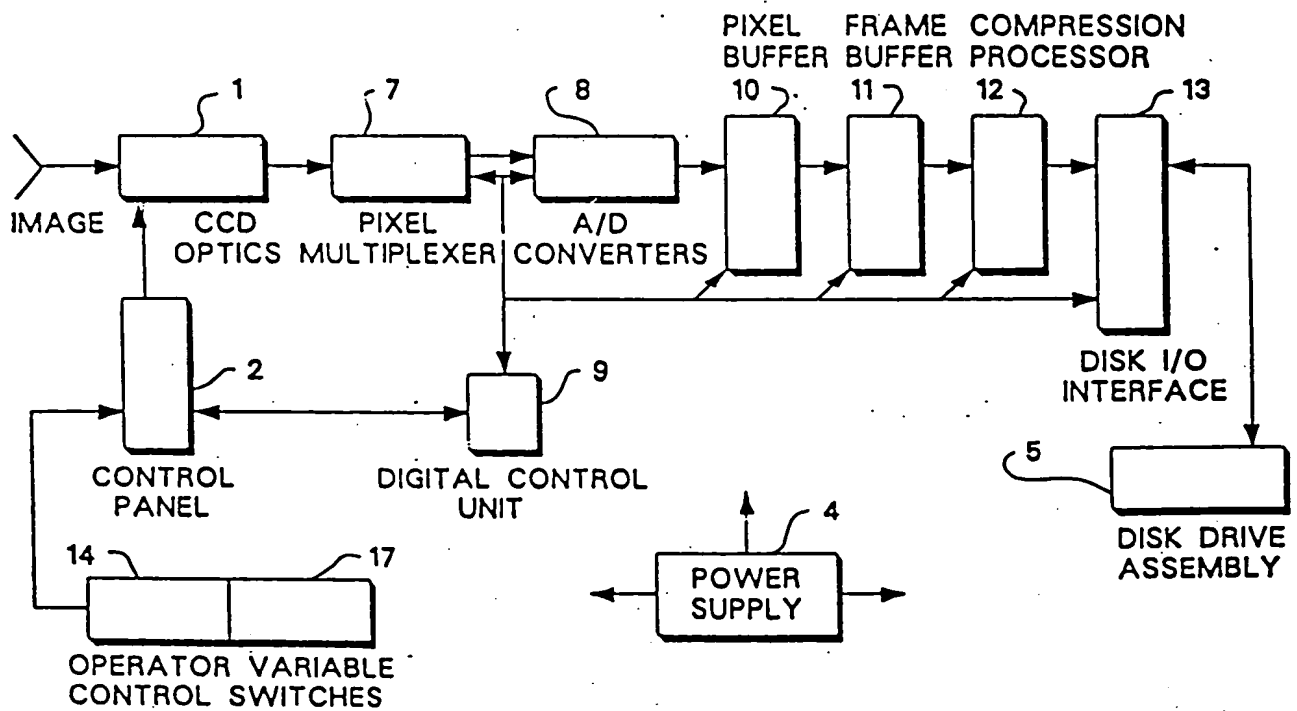


FIG. 2

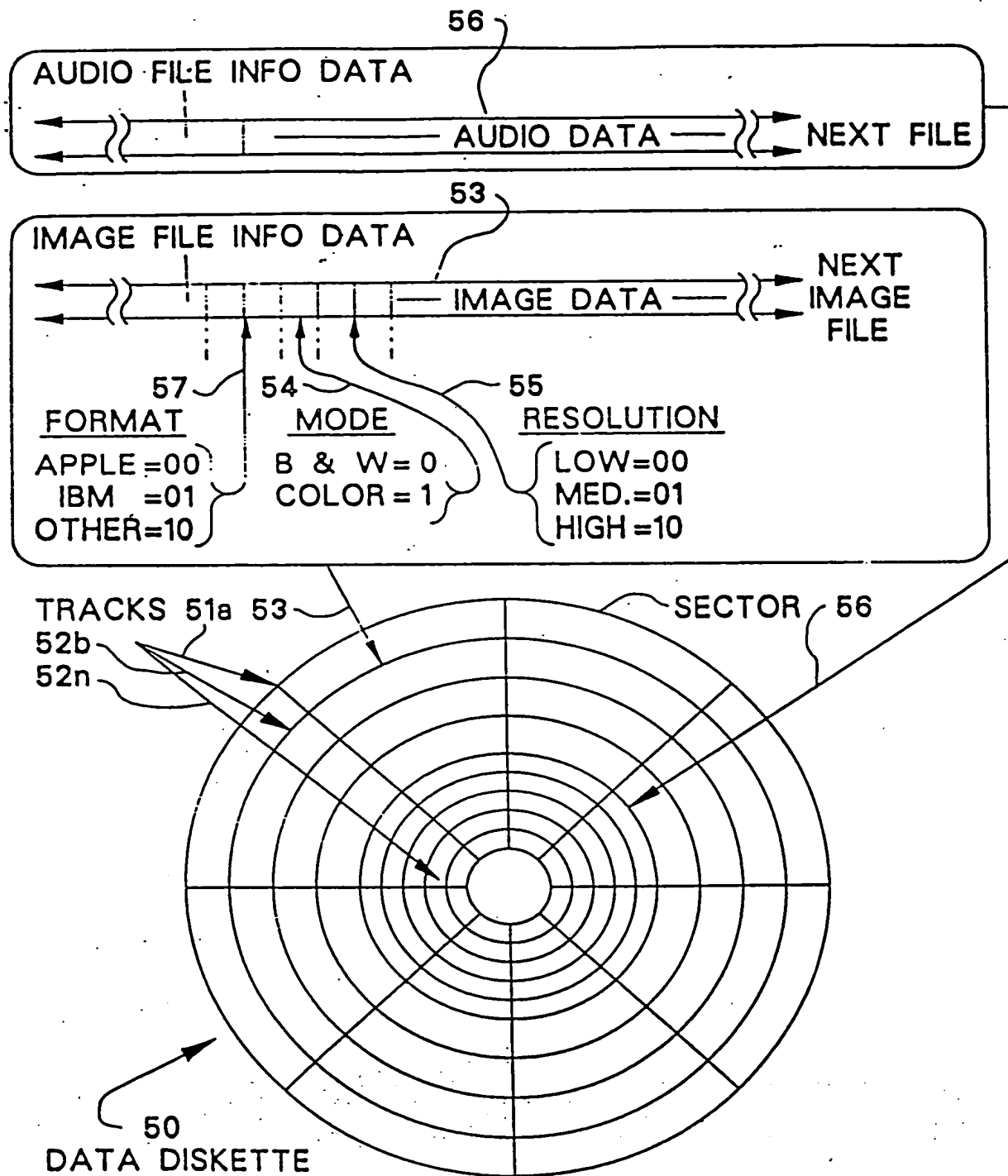


FIG. 2A

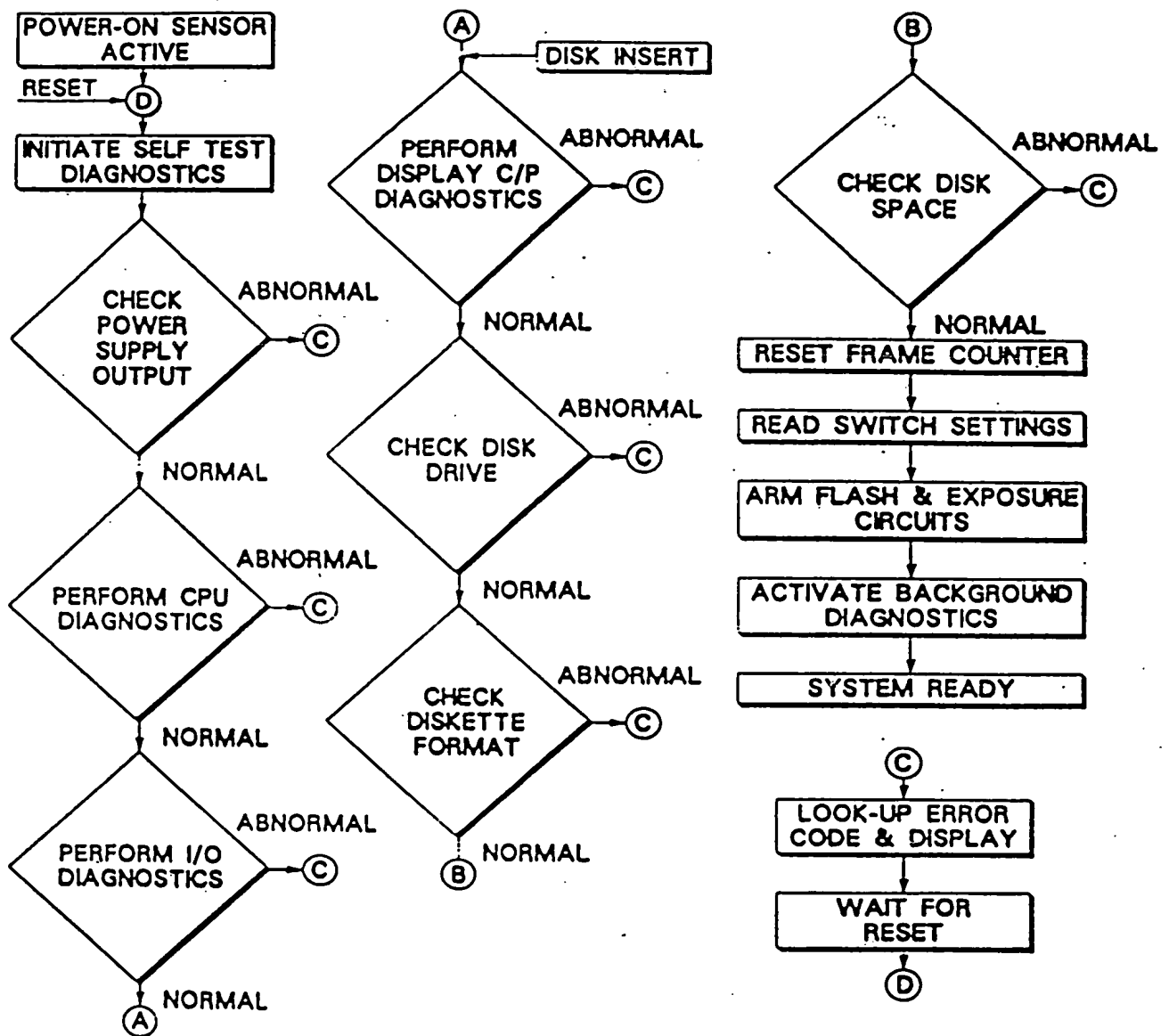


FIG. 3

FIG. 5 A

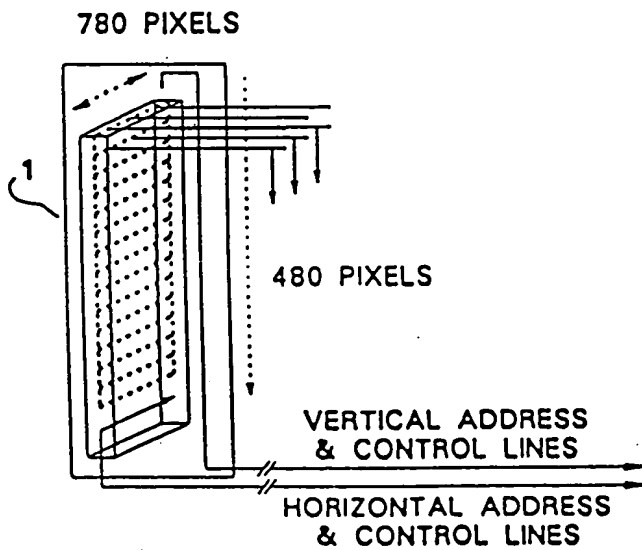
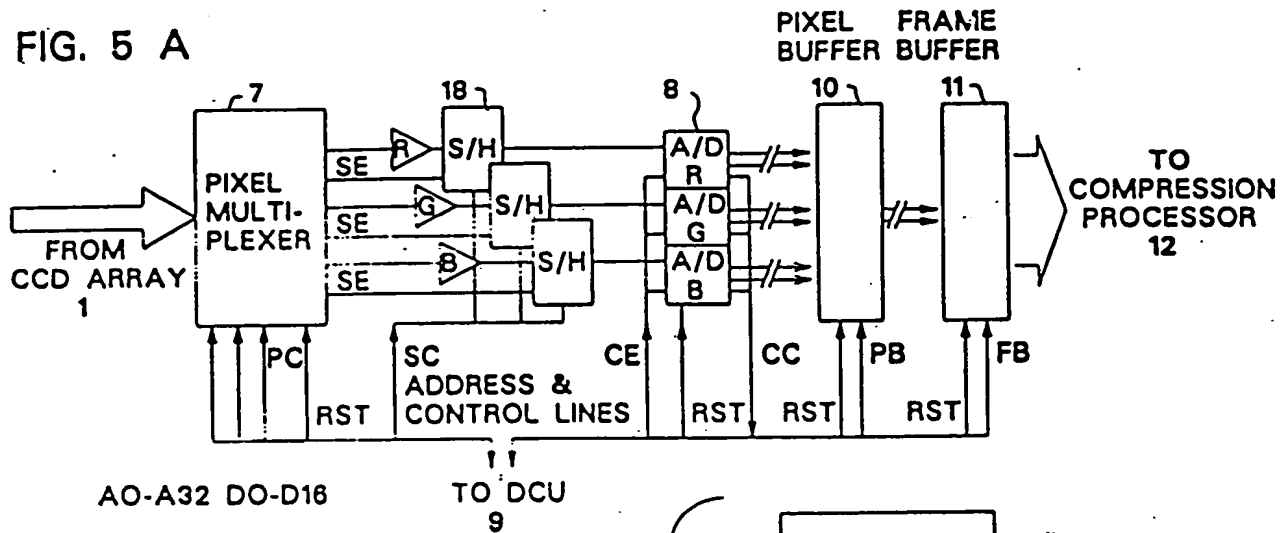
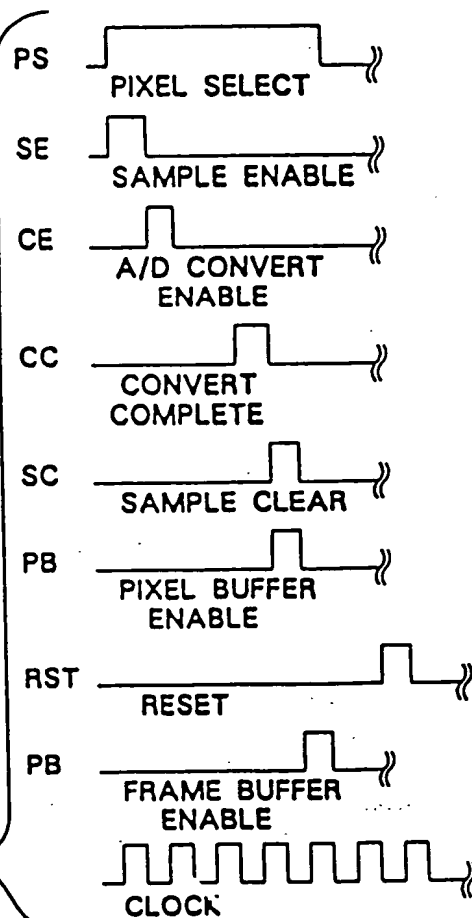


FIG. 4

FIG. 5B



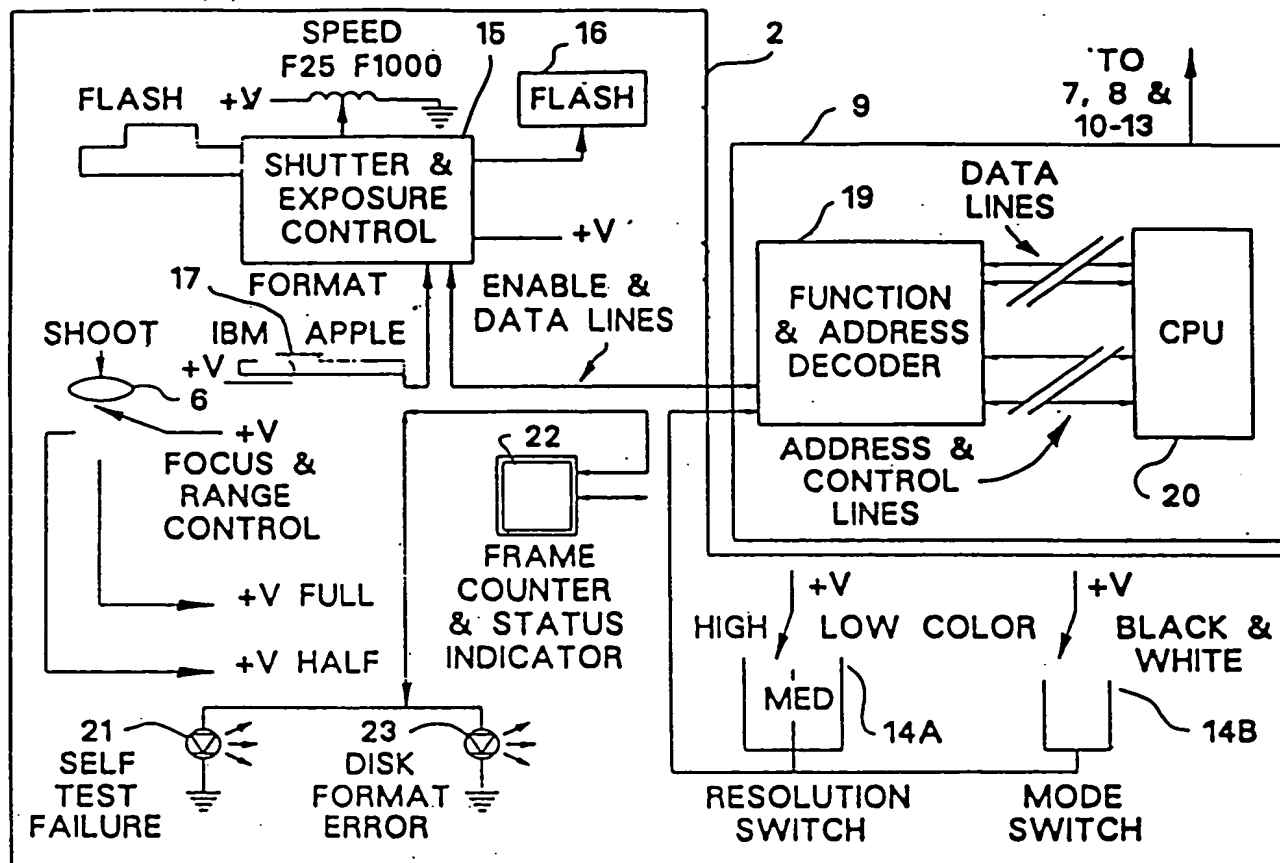


FIG. 6

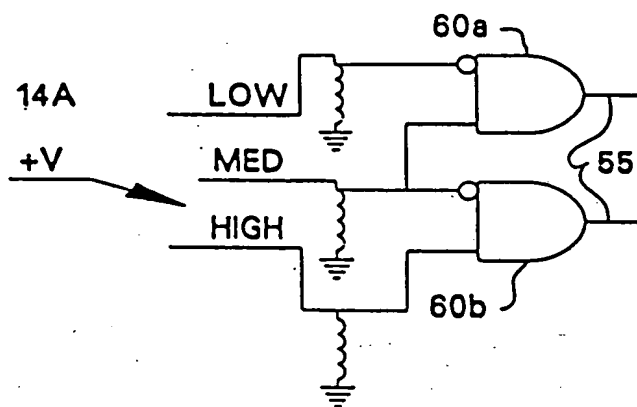


FIG. 6A

512-BYTE HEADER
plcSIZE
plcFRAME
OPCODE
PICTURE DATA
⋮
OPCODE
PICTURE DATA END OF PICTURE

FIG.6B

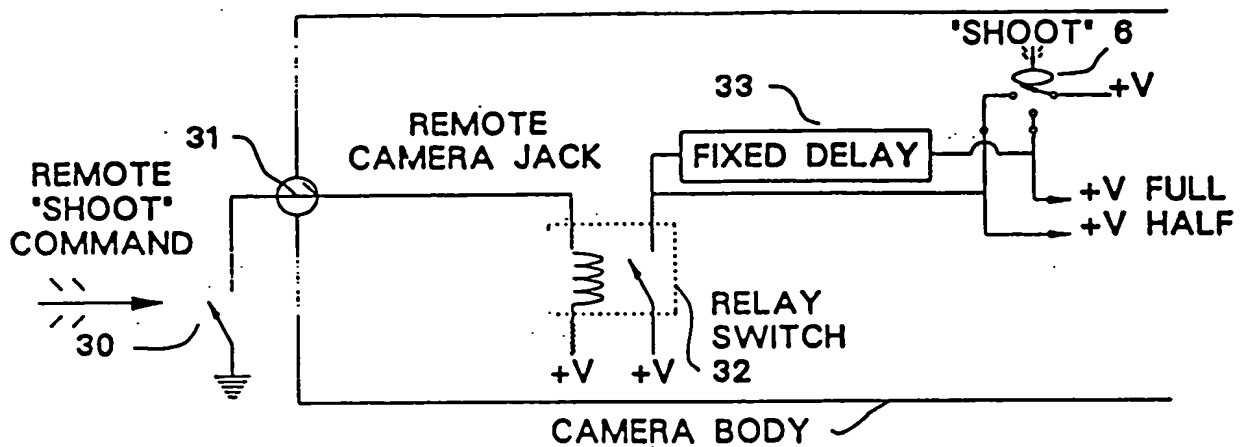


FIG. 6C

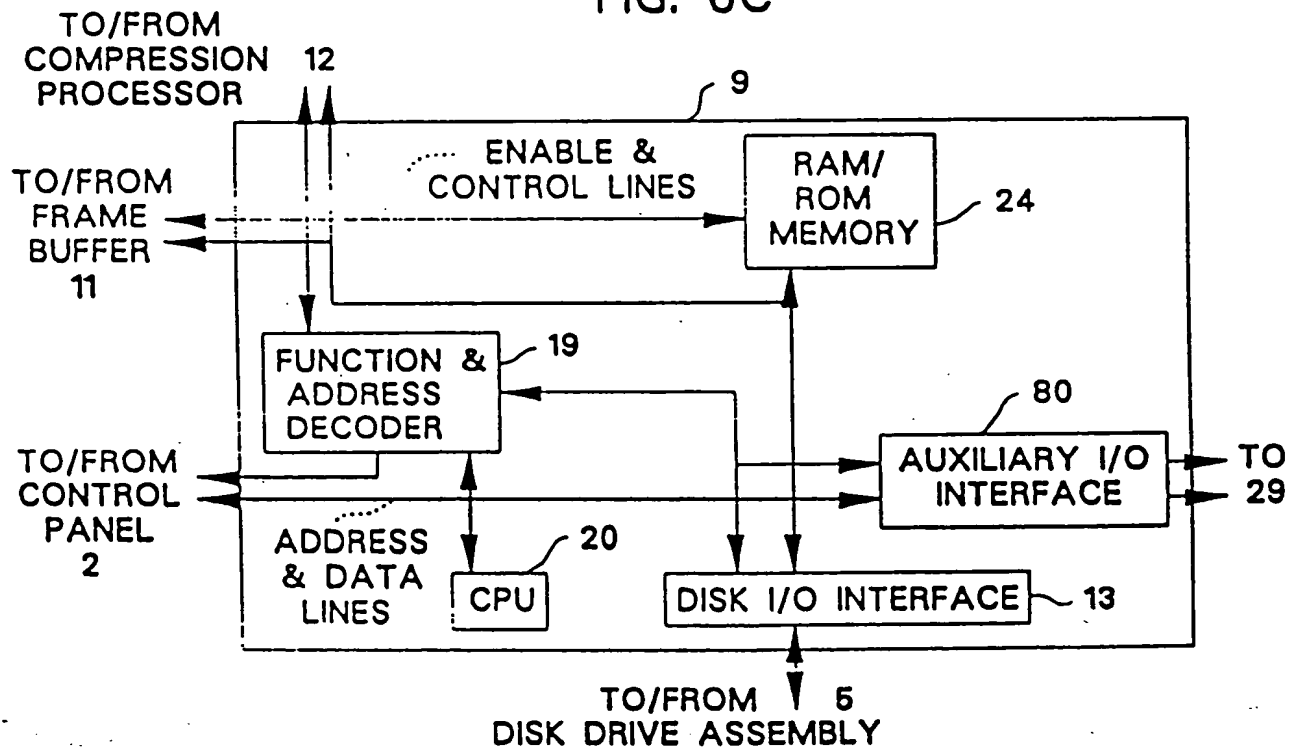


FIG. 7

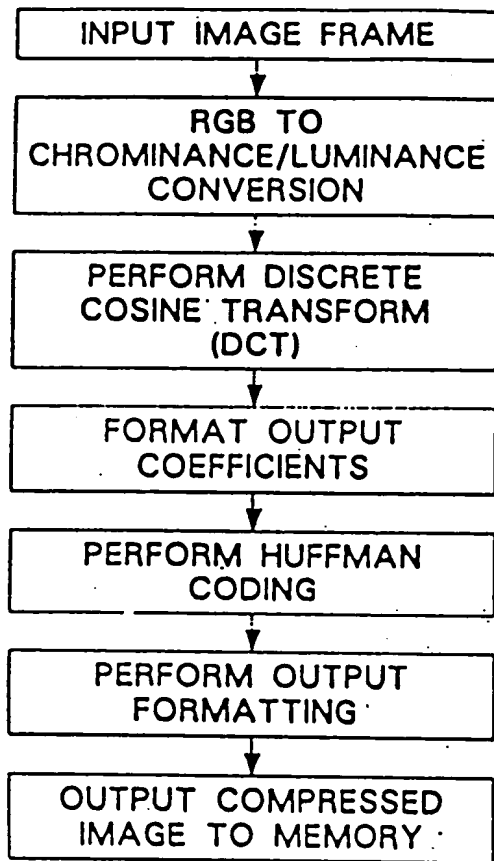


FIG. 8

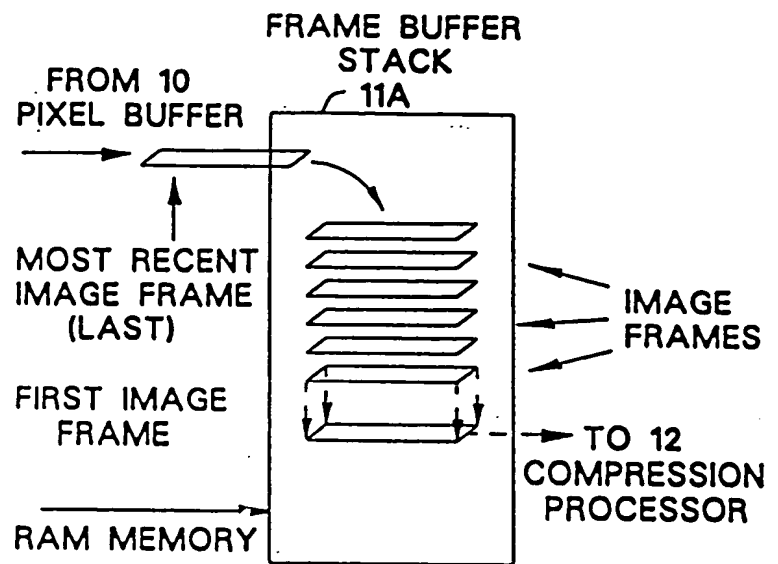


FIG. 13

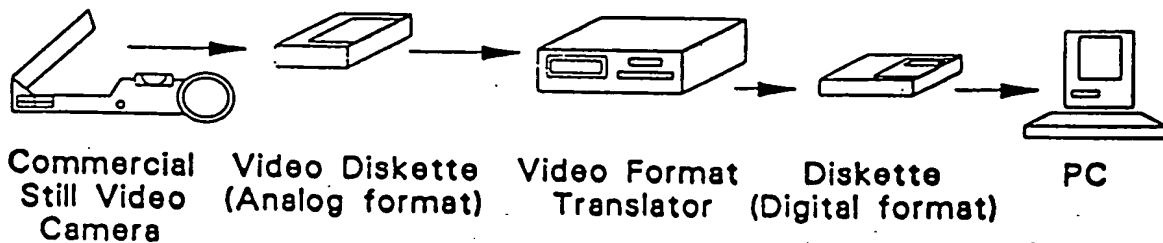


FIG. 10

FIG. 9 is a block diagram of a video processing system. The system includes a 2 inch disk drive assembly (26) connected to a pixel mux (40-7). The pixel mux is connected to a pixel buffer (40-10) and a frame buffer (40-11). The pixel buffer is connected to a compression processor (40-12). The frame buffer is connected to a disk I/O interface (40-13). The compression processor is connected to a disk I/O interface (40-13). The disk I/O interface is connected to a 3 1/2 inch disk drive assembly (40-5). The system also includes a digital control unit (40-9) connected to a control panel & display (40-2) and operator variable control switches (40-14). The control panel & display is connected to the pixel mux (40-7) and the frame buffer (40-11). The operator variable control switches are connected to the pixel buffer (40-10) and the frame buffer (40-11). A power supply (40-4) is connected to the compression processor (40-12) and the disk I/O interface (40-13).

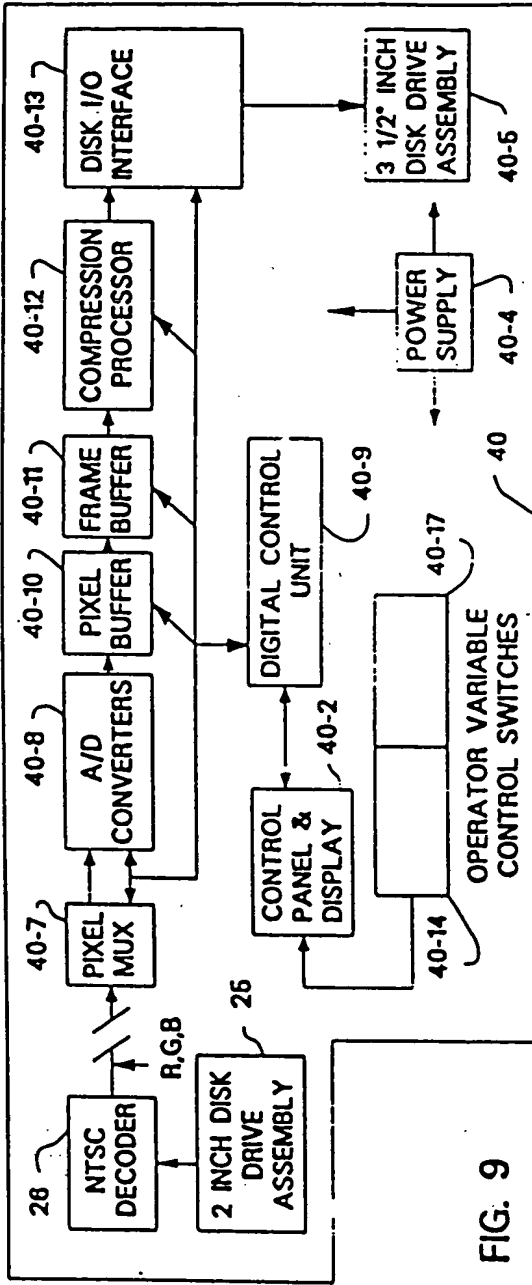


FIG. 9

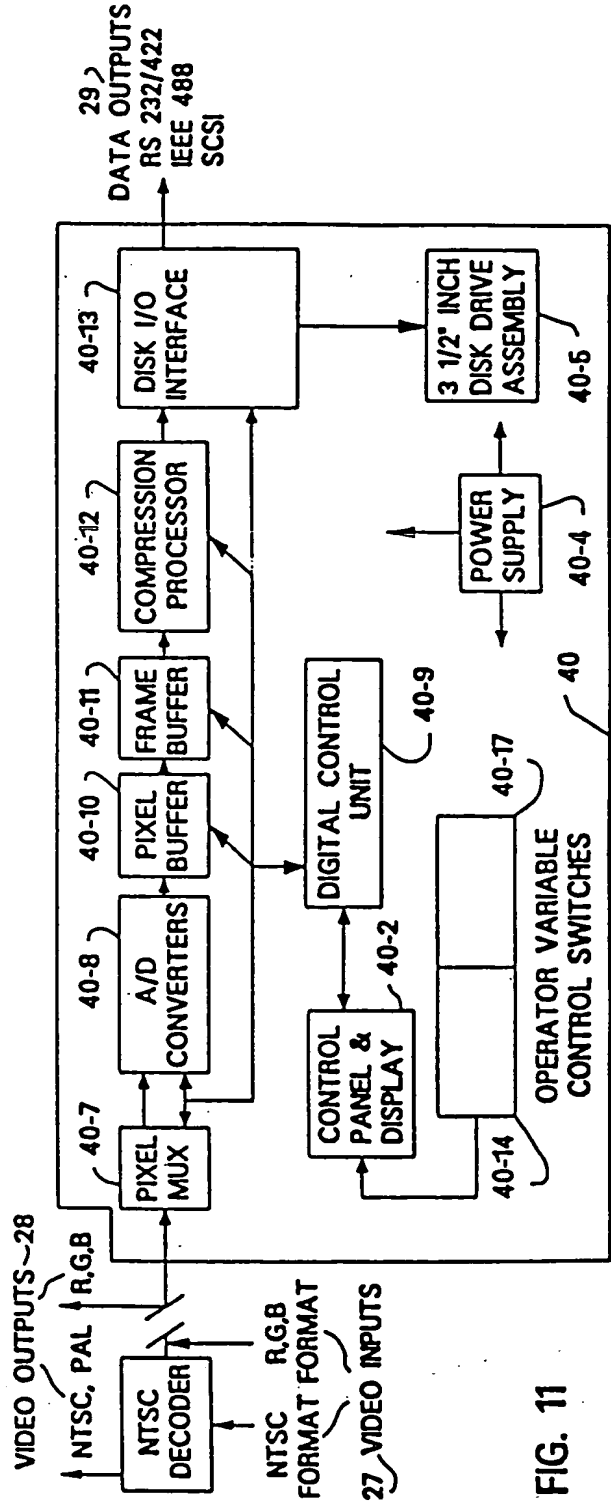


FIG. 11

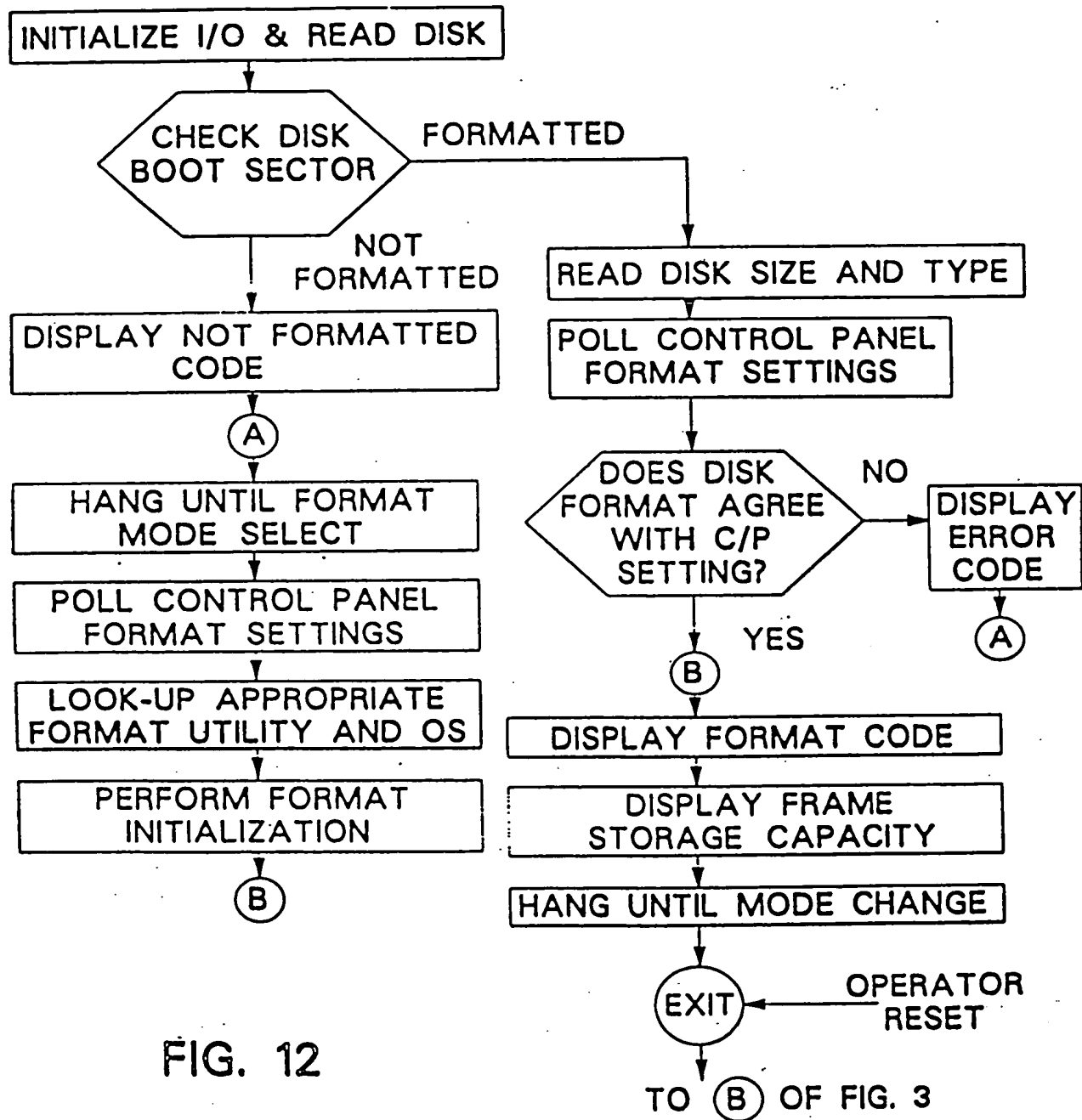


FIG. 12

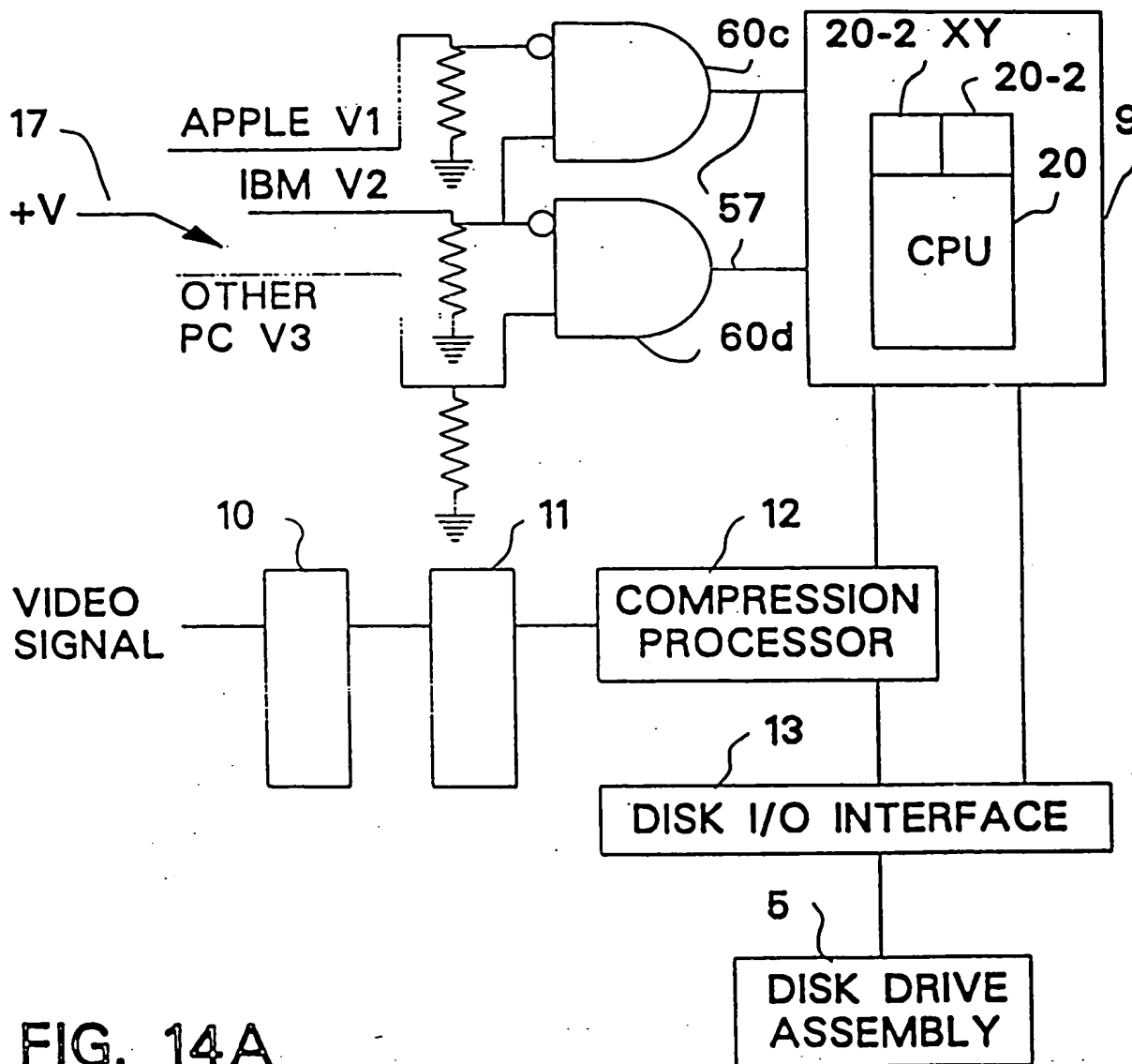


FIG. 14A

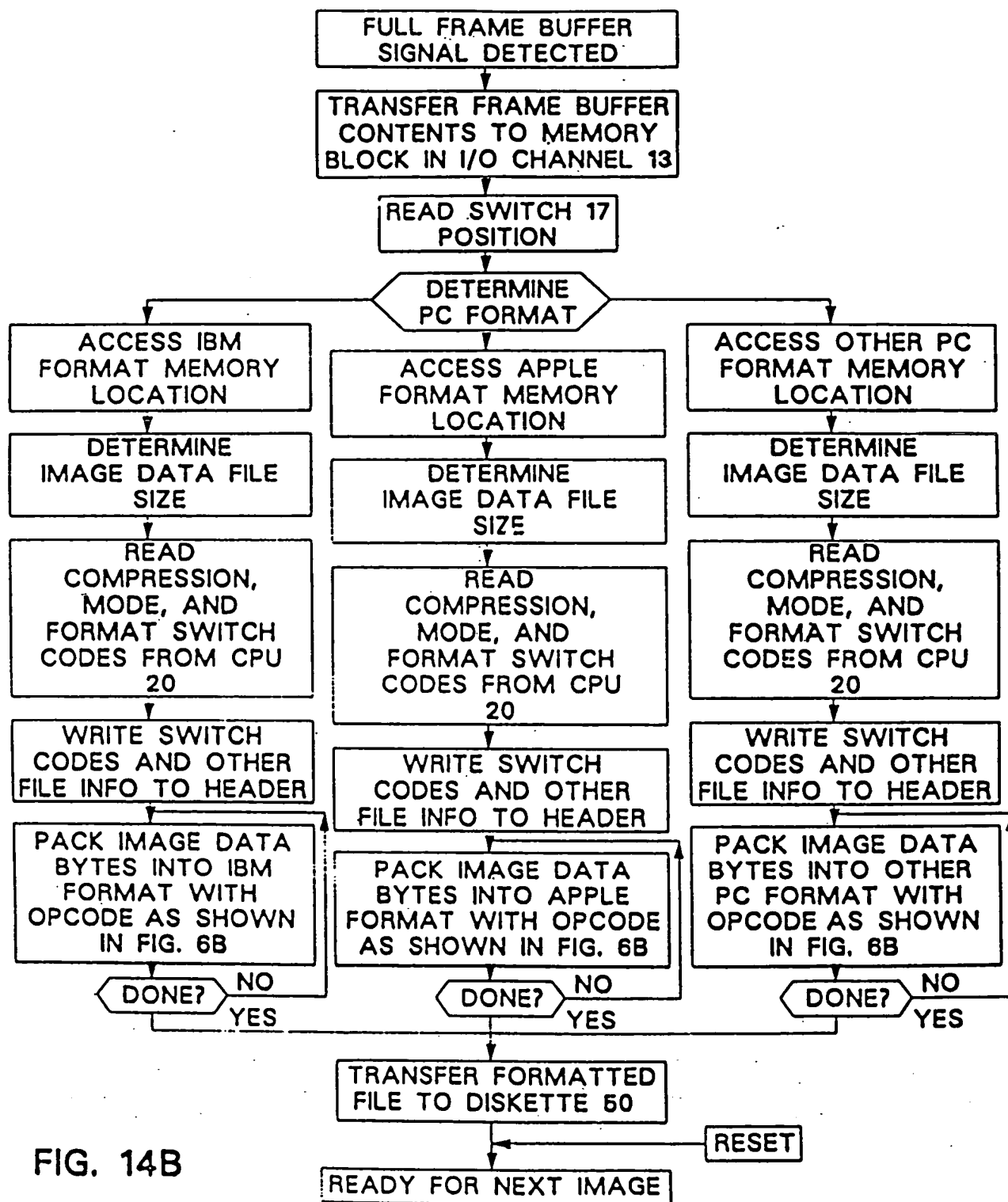


FIG. 14B